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TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURING METHOD

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ABSTRACT:

PROBLEM TO BE SOLVED: To improve the NBTI life of a device by reducing hydrogen content in a silicon nitride film covering a gate electrode.

SOLUTION: A CVD device 100 which is used for deposition of a silicon nitride film has a structure wherein a hot wall furnace 103 for thermally decomposing source gas and a chamber 101 for forming a film on a surface of a wafer 1 are isolated from each other. The hot wall furnace 103 for thermally decomposing the source gas is arranged above the chamber 101, and a heater 104 which can set the inside of the furnace to a high temperature atmosphere whose maximum temperature is almost 1200°C is installed on the outer periphery of the hot wall furnace 103. The source gas which is supplied to the hot wall furnace 103 through pipes 105, 106 is thermally decomposed previously in the furnace, and its decomposed component is supplied above a stage 102 of the chamber 101 and forms a film on the surface of the wafer 1.

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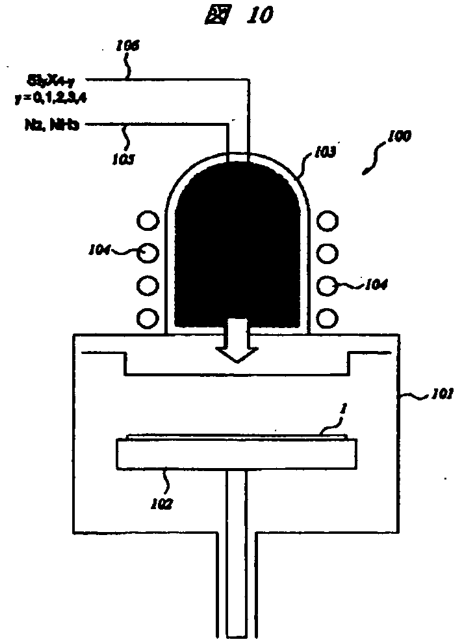
(54)【発明の名称】　半導体集積回路装置およびその製造方法

(57)【要約】
【課題】　ゲート電極を覆う窒化シリコン膜中の水素含有量を低減することによって、デバイスのＮＢＴＩ寿命を向上させる。
【解決手段】　窒化シリコン膜の堆積に使用するＣＶＤ装置１００は、ソースガスを熱分解するホットウォール炉１０３と、ウエハ１の表面に膜を形成するチャンバ１０１とが互いに分離された構造になっている。チャンバ１０１の上方には、ソースガスを熱分解するためのホットウォール炉１０３が設けられており、その外周には、炉内を最高１２００℃程度の高温雰囲気に設定できるヒータ１０４が設置されている。配管１０５、１０６を通じてホットウォール炉１０３に供給されたソースガスは、この炉内であらかじめ熱分解され、その分解成分がチャンバ１０１のステージ１０２上に供給されてウエハ１の表面に膜を形成する。

図 10



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention is applied to the semiconductor integrated circuit equipment which has the process which deposits a silicon nitride film on a substrate especially using the CVD (Chemical Vapor Deposition) method about semiconductor integrated circuit equipment and its manufacturing technology, and relates to effective technology.
[0002]
[Description of the Prior Art] In the manufacture process of LSI that detailed-izing in recent years and high integration progressed, forming an isolation slot (Shallow Groove Isolation;SGI) in a silicon substrate, or forming a contact hole in it by self-adjustment (self aryne) to the gate electrode of MISFET (Metal Insulator Semiconductor Field Effect Transistor) is performed by using the etch-rate difference of a silicon-oxide film and a silicon nitride film. About the formation method of such an isolation slot (SGI), JP,11-16999,A etc. has a publication, for example. Moreover, about the formation method of self aryne contact (Self Align Contact;SAC), JP,11-17147,A etc. has a publication, for example.
[0003] Although the silicon nitride film used at the above-mentioned formation process of an isolation slot and the above-mentioned formation process of self aryne contact is formed of the CVD which generally used silane system gas, ammonia (NH3), or nitrogen (N2), such as a mono silane (SiH4), for source gas, in this silicon nitride film, it is known that a lot of hydrogen originating in source gas will be incorporated.
[0004] If the silicon nitride film used as the stopper film of self aryne contact is deposited on the upper part or the side containing p type polycrystal silicon film of a gate electrode, the boron (B) which is a dopant in p type polycrystal silicon film would diffuse JP,2000-58483,A (crests) in the gate insulator layer or the silicon substrate, and it will have pointed out the problem of fluctuating flat band voltage (Vfb) and threshold voltage (Vth), or degrading the reliability of a gate insulator layer. It is supposed that it is such a problem the cause which the hydrogen of the material gas origin included in a silicon nitride film makes increase diffusion of boron (enhanced diffusion).
[0005] This official report deposits a silicon nitride film as a cure which solves the above-mentioned problem using the source gas which does not contain hydrogen, and is indicating the technology which suppresses the enhanced diffusion of boron by reducing the hydrogen concentration in a film less than to 1x1021 atom/cc. The halogenated compound of silicon like SiF4, SiCl4, SiBr4, and SiI4 as source gas and the mixed gas of nitrogen which do not contain hydrogen are illustrated.
[0006] Since a lot of hydrogen in a film is incorporated, when the silicon nitride film which deposited JP,2000-114257,A (Muraoka et al.) by the plasma CVD method which used a mono silane (SiH4) and nitrogen uses this film for a gate insulator layer, the problem that bad influences, such as hot carrier degradation of MISFET (MetalInsulator Semiconductor Field Effect Transistor) and leakage-current increase, arise is pointed out. Since a halogen is incorporated in large quantities on the other hand although hydrogen is not incorporated in a film when it replaces with a mono silane and the halogenated compound of silicon like SiF4 is used, the problem of bringing about the increase in a trap site has been pointed out.
[0007] This official report is indicating the technology in which the content of hydrogen or a halogen forms a low silicon nitride film, by exciting at least one side of 2 silicon fluorides (SiF2) and nitrogen, and supplying a substrate as a cure which solves the above-mentioned problem. As a method of obtaining the excited 2 silicon fluorides, 4 silicon fluorides (SiF4) are electrically excited by the microwave discharge, or the method of contacting the lump of Si which heated and making [it is / 4

decomposition temperature / of source gas / vertical axis] in a film is expressed.
[0053] As for desorption of hydrogen, a peak is accepted like illustration near 400 degree C and near 750 degrees C - 800 degree C. It is thought that the hydrogen in a silicon nitride film exists as Si-H combination and N-H combination, since Si-H combination has binding energy smaller than N-H combination, the desorption near 400 degree C originates in Si-H combination, and the desorption near 750 degrees C - 800 degree C is presumed to be a thing resulting from N-H combination.
[0054] The temperature of the heater 104 at the time of pyrolyzing source gas in the hot-wall furnace 103 of aforementioned CVD system 100 from this measurement result should make the minimum near 600 degree C where the maceration of N-H coupling is promoted, and since many intermediate-field impurities which contained N-H coupling at the temperature not more than it will be generated, it is not practical. In order to reduce the amount of generation of an intermediate-field impurity including N-H combination, it is desirable to make temperature of a heater 104 into 700 degrees C or more, it considers as 800 degrees C or more more preferably, and Si-H combination and N-H combination are made to dissociate nearly completely.
[0055] Since it dissociates with the hot-wall furnace 103, the chamber 101 which is the membrane formation processing section on the other hand can lower the temperature of the stage 102 in which a wafer 1 is carried to below a room temperature, even when the temperature of a heater 104 is set as 800 degrees C or more. Moreover, since it has the cold-wall structure of heating only the wafer 1 on a stage 102, even if a chamber 101 sets the temperature of a stage 102 as low temperature, the fall of the throughput of membrane formation has them. [few]
[0056] Although it is before and after 0 degree C, since it has a possibility of the throughput of membrane formation falling, or it being cooled as the intermediate field of the source gas generated in the hot-wall furnace 103 arrive at the front face of a wafer 1, and generating an impurity when the practical minimum temperature of the stage 102 at the time of membrane formation has the too low temperature of a stage 102, you should make it preferably 400 degrees C or more. Although the upper limit temperature of a stage 102 is the temperature of the upper limit permitted, and it cannot generally be ******(ed) on the property of the device formed in the principal plane of a wafer 1 since it changes with devices, in the DRAM mixed loading LSI of this operation gestalt, it is 700 degrees C - 750 degrees C, for example. if the temperature of a stage 102 exceeds this upper limit temperature -- B in the polycrystal silicon film 11 (boron) -- n type -- it is spread in a well 9 and there is a possibility of changing the threshold voltage of p-channel type MISFET which constitutes a part of logical circuit
[0057] Moreover, although it should be carried out to more than 0.013kPa(s) (0.1Torr) at least, when the throughput of membrane formation is taken into consideration, it is usually desirable [the pressure of source gas] to consider as 45.5kPa (350Torr) order. On the other hand, when the safety of source gas etc. is taken into consideration, as for the upper limit of gas pressure, it is desirable to carry out to below 98.8kPa (760Torr).
[0058] The source gas used for formation of a silicon nitride film 14 It is not what is restricted to the combination of the above-mentioned dichloro silane (SiH2Cl2) and ammonia (NH3). Generally it is SiHyX (4-y) (X), such as the known source gas 4 currently used for formation of the silicon nitride film using reduced pressure CVD (LP-CVD) equipment, for example, SiH, and Si2H6. Halogens, such as F, Cl, Br, and I, and y can use what combined the silicon compound shown by 0, 1, 2, 3, or 4, and NH3, N2H4 or N2.
[0059] The hydrogen concentration in a silicon nitride film can be further reduced by using what combined the source gas, SiF4 and SiCl4, which does not contain hydrogen in a molecule among the above-mentioned silicon compounds, Si2Cl6, a silicon compound like SiBr4 and SiI4, and N2. [for example,] Although a step coverage falls a little compared with the case where the source gas containing hydrogen is used, into a molecule when these silicon compounds are used, since a silicon nitride film 14 is deposited on the front face of a flat ground, trouble does not have it.
[0060] Thus, since source gas can be pyrolyzed at the elevated temperature of 800 degrees C or more by using above-mentioned CVD system 100, the hydrogen concentration in a film can obtain the low silicon nitride film 14 extremely. Moreover, since the temperature of the wafer 1 under membrane formation (substrate) can be set as low temperature, property change of the device by the thermal load can be suppressed certainly.
[0061] Next, as shown in <u>drawing 12</u> , by using the photoresist film 61 as a mask and carrying out dry etching of a silicon nitride film 14, the W film 13, the WNX film 12, and the polycrystal silicon film 11 one by one, gate electrode 11a (word line WL) is formed on the gate insulator layer 10 of a DRAM

mask -- using -- p type -- the polycrystal silicon film 11 of the upper part of a well 8 -- P (Lynn) -- an ion implantation -- carrying out -- n type -- the ion implantation of the B (boron) is carried out to the polycrystal silicon film 11 of the upper part of a well 9 thereby -- the conductivity type of the polycrystal silicon film 11 -- p type -- the upper part of a well 8 -- n type -- becoming -- n type -- it becomes p type in the upper part of a well 9 This ion implantation is performed in order to use as a surface channel type each of n channel type MISFET which constitutes a logical circuit, and p-channel type MISFET.

[0046] Next, after washing the front face of the polycrystal silicon film 11 by fluoric acid, as shown in drawing 8 , the WNX film 12 of about 7nm of thickness and the W film 13 of about 70nm of thickness are continued and deposited on the upper part of the polycrystal silicon film 11 by the sputtering method. The WNX film 12 functions as a barrier layer which prevents the polycrystal silicon film 11 and the W film 13 reacting at the process which heat-treats a substrate 1. In addition, it may replace with the W film 13 and Mo (molybdenum) film may be deposited on the upper part of the WNX film 12. Moreover, it can replace with the polycrystal silicon film 11, and the silicon film which contained germanium (germanium) 5% to about 50% can also be used. When germanium is included in silicon, it is narrow, a bird clapper and the solid-solution limit community of an impurity are high, the band gap of silicon originates in a bird clapper, and there is an advantage on which contact resistance with the upper WNX film 12 is reduced. In order to include germanium in silicon, there is the method of depositing the silicon film which contained germanium by the CVD using a mono silane (SiH4) and GeH4 outside the method of carrying out the ion implantation of the germanium to a silicon film.

[0047] Next, as shown in drawing 9 , the silicon nitride film 14 of about 160nm of thickness is deposited on the upper part of the W film 13 in CVD. This silicon nitride film 14 is used considering the upper surface of the gate electrode formed at a next process as a wrap cap insulator layer. With this operation gestalt, this silicon nitride film 14 is deposited using the following equipments.

[0048] Drawing 10 is the schematic diagram showing the principal part of CVD system 100 used for deposition of a silicon nitride film 14. The stage 102 in which a wafer (substrate) 1 is carried is established in the center section of the chamber 101 of this CVD system 100. The heater (not shown) heated at the temperature which asks for a wafer 1 is built in this stage 102. That is, the chamber 101 of this CVD system 100 has the cold-wall structure of heating only the wafer 1 on a stage 102 instead of the hot-wall structure where the whole interior is heated by uniform temperature. Since the pyrolysis component of source gas hardly deposits the cold-wall type chamber 101 on a wall, high membrane formation of a throughput is possible for it. Moreover, since the sheet method which forms membranes by carrying one wafer 1 at a time on a stage 102 is adopted, in comparison with the batch-type heat CVD system, the chamber 101 of this CVD system 100 can set up the temperature of a wafer 1 with high precision, and its thickness homogeneity in a wafer side is good.

[0049] In addition, since it is indicated by the Japanese patent application No. (Japanese filing-date-of-application October 31, 2000) 332863 [2000 to] by this invention persons, the Japanese patent application No. (Japanese filing-date-of-application July 31, 2000) 232191 [2000 to], etc. about the newest single-wafer-processing silicon-nitride CVD furnace and this newest method, those publications are not repeated here.

[0050] The hot-wall furnace 103 for pyrolyzing source gas is formed above the above-mentioned chamber 101. The hot-wall furnace 103 consists of heat-resisting material, such as a quartz, and the heater 104 which can set the inside of a furnace as about a maximum of 1200-degree C elevated-temperature atmosphere is installed in the periphery. The source gas supplied to the hot-wall furnace 103 through piping 105 and 106 is beforehand pyrolyzed in this furnace, and the decomposition component is supplied on the stage 102 of a chamber 101, and it forms a film in the front face of a wafer 1. Source gas is for example, a dichloro silane (SiH2Cl2) and ammonia (NH3).

[0051] Thus, since the hot-wall furnace (heat-treatment section) 103 which pyrolyzes source gas, and the chamber (membrane formation processing section) 101 which forms a film in the front face of a wafer 1 have structure separated mutually, above-mentioned CVD system 100 can control independently the decomposition temperature of source gas, and the temperature of a wafer 1.

[0052] It is the graph which shows the result which evaluated the desorption behavior of the hydrogen in the silicon nitride film which drawing 11 used a dichloro silane (SiH2Cl2), ammonia (NH3), and a mono silane (SiH4) and nitrogen (N2) for source gas, and was deposited using the commercial low pressure CVD system using the temperature programmed desorption (Thermal Desorption Spectrometry;TDS), and the ionic strength of the hydrogen [can set a horizontal axis and /

method, the field of left-hand side and a center shows a DRAM formation field, and the right-hand side field shows the logical-circuit formation field.

[0039] First, the semiconductor substrate which consists of p type single crystal silicon which has about [1-10ohmcm] specific resistance as shown in drawing 1 (henceforth a substrate) moreover, it may be called a wafer -- after forming the silicon-oxide film (pad oxide film) 2 aiming at stress relief and active field protection in the principal plane of a substrate 1 by oxidizing 1 thermally at 800-850 degrees C, a silicon nitride film 3 is deposited on the upper part of the silicon-oxide film 2 in CVD

[0040] The above-mentioned silicon nitride film 3 is deposited by the reduced pressure CVD (LP-CVD) which used a dichloro silane (SiH2Cl2), ammonia (NH3), or a mono silane and nitrogen (N2) for source gas. Moreover, since a silicon nitride film 3 needs comparatively thick thickness (for example, 120nm), it is desirable by using the batch-type heat CVD system equipped with the hot-wall furnace, for example, processing simultaneously 50 sheets to about 100 substrates 1 to raise the throughput of membrane formation. The method (radiation heating at the heater besides a tube wall) which heats a wafer indirectly is used for a hot-wall type heat CVD system, and it has the structure of heating the wall of a chamber (reaction chamber), and the whole atmosphere in a chamber to the temperature more than the decomposition temperature of source gas.

[0041] In case the above-mentioned silicon nitride film 3 is deposited, it is desirable to pyrolyze source gas at the elevated temperature of 800 degrees C or more. Since Si-H coupling and N-H coupling which are contained in source gas are dissociated nearly completely when source gas is pyrolyzed at the elevated temperature of 800 degrees C or more, the very few silicon nitride film 3 of a hydrogen content is obtained. Since the amount of the hydrogen diffused in a substrate 1 from a silicon nitride film 3 at the time of heat treatment performed at the formation process of the isolation slot mentioned later by this can be extremely made into a low, change of the element property by the hydrogen which remained to the substrate 1 can be suppressed certainly.

[0042] Next, as shown in drawing 2 , the silicon nitride film 3 and the silicon-oxide film 2 of an isolation field are removed by the dry etching which used the photoresist film 60 as the mask. Then, after removing the photoresist film 60, as shown in drawing 3 , the silicon-oxide film 5 is formed in the wall of the isolation slot 4 by forming the isolation slot 4 with a depth of about 350nm and oxidizing a substrate 1 thermally to the substrate 1 of an isolation field at about 950 degrees C continuously by the dry etching which used the silicon nitride film 3 as the mask. The silicon-oxide film 5 is formed in order to ease the stress of the silicon-oxide film 5 embedded to the interior of the isolation slot 4 at the following process, while recovering the etching damage produced in the wall of the isolation slot 4.

[0043] Next, as shown in drawing 4 , after depositing the silicon-oxide film 7 and heat-treating a substrate 1 at about 1000 degrees C continuously by CVD on the principal plane of a substrate 1 and improving the membraneous quality of the silicon-oxide film 7, the silicon-oxide film 7 is ground using the chemical machinery grinding (Chemical Mechanical Polishing;CMP) method, and flattening of the front face is carried out. This polish uses the aforementioned silicon nitride film 3 for a stopper, and leaves the silicon-oxide film 7 only to the interior of the isolation slot 4. According to the process so far, the isolation slot 4 is completed to the principal plane of a substrate 1. As shown in drawing 5 , the active field L of a large number which have the pattern of the shape of a long and slender island with which the circumference was surrounded by the isolation slot 4 is formed in the substrate 1 of a DRAM formation field by forming the above-mentioned isolation slot 4. In addition, the field on the left-hand side of drawing 4 (and each cross section explaining the manufacture method) is the cross section which met the A-A line of drawing 5 , and a central field is the cross section which met the B-B line.

[0044] next, after removing the silicon nitride film 3 which remained on the principal plane of a substrate 1 by the heat phosphoric acid, it is shown in drawing 6 -- as -- a part of substrate 1 -- B (boron) -- an ion implantation -- carrying out -- p type -- a well 8 -- forming -- other parts -- P (Lynn) -- an ion implantation -- carrying out -- n type -- a well 9 is formed then, the thing done for the wet oxidation of the substrate 1 at about 850 degrees C after removing the silicon-oxide film 2 which remained in the front face of a substrate 1 by fluoric acid -- p type -- the front face of a well 8, and n type -- the gate insulator layer 10 which consists of a pure silicon-oxide film of about 6nm of thickness is formed in the front face of a well 9 The gate insulator layer 10 may be replaced with a silicon-oxide film, and may be formed by the compound insulator layer of an acid silicon nitride film, a silicon nitride film, a silicon-oxide film, and a silicon nitride film etc.

[0045] next, the photoresist film (not shown) as shown in drawing 7 , after depositing the polycrystal silicon film 11 of about 70nm of thickness on the upper part of the gate insulator layer 10 in CVD -- a

includes the following processes. (a) The process which introduces into the plasma-treatment section the source gas containing the 1st gas which has silicon in a molecule, and the 2nd gas which has nitrogen in a molecule, supplies the gas containing the decomposition product of the process which carries out plasma treatment of the aforementioned source gas, the above 1st generated in the (b) aforementioned plasma-treatment section, and the 2nd gas to the membrane-formation processing section, and deposits the 1st insulator layer which makes the 1st silicon nitride film a principal component on the principal plane of a semiconductor wafer.
[0029] Moreover, the manufacture method of the semiconductor integrated circuit equipment of this invention makes more preferably concentration of the hydrogen contained in the 1st silicon nitride film of the above three or less 0.5x1021 atoms/cm three or less 1x1021 atoms/cm three or less 2x1021 atoms/cm.
[0030] In addition, in this application, especially when calling it semiconductor integrated circuit equipment, not only except for what is made on a single-crystal-silicon substrate but except for the case where the purport which is not so is specified especially, what is made on other substrates like a SOI (Silicon On Insulator) substrate or the substrate for TFT (Thin Film Transistor) liquid crystal manufacture shall be included. Moreover, a wafer means an insulation of the single-crystal-silicon substrate (general almost disk form) used for manufacture of semiconductor integrated circuit equipment, a SOI substrate, a glass substrate, and others, a half-insulation or a semiconductor substrate, and the substrate that compounded them.
[0031] moreover, that from which not only a stoichiometry-thing but composition shifted in this application except for what carried out purport designation not right [that] especially when calling it SiN, Si3N4, a silicon nitride, a silicon nitride, a silicon nitride, etc., i.e., nitrogen, -- a rich thing and silicon -- a rich thing and the thing containing other elements, for example, the thing currently called [in / semiconductor industry / usually / thing / considerable-amount ****] / such in hydrogen, shall be included
[0032] Moreover, the hydrogen concentration in the silicon nitride film specified by this invention shall say the concentration when measuring the hydrogen contained in the film immediately after membrane formation (as depo) by FTIR (Fourier transform type infrared spectrophotometer).
[0033] Moreover, when calling it a NBTI life, where negative bias is impressed to a gate electrode, it is left at 85 degrees C, and what computed the life cycle from the shift amount per time of threshold voltage is said.
[0034] When calling it a cold-wall type CVD system, it is the CVD system of a method (resistance heating, high-frequency induction heating, or lamp heating) which generally heats a wafer to temperature higher than the inner circle wall of a chamber, and what does not use plasma etc. directly is said.
[0035] Furthermore, in the gestalt of the following operations, when the number of elements etc. is mentioned (the number, a numeric value, an amount, the range, etc. are included) and it shows clearly especially, you may be not the thing limited to the specific number except for the time of being theoretically limited to a specific number clearly but more than a specific number, or the following. Furthermore, in the gestalt of the following operations, especially the component (an element step etc. is included) cannot be overemphasized by that it is not necessarily indispensable except for the case where it is thought theoretically that it is clearly indispensable, when shown clearly.
[0036] When similarly mentioning configurations, such as a component, physical relationship, etc. and it especially shows clearly in the gestalt of the following operations, the case where it thinks clearly theoretically shall be removed, and what approximates or is substantially similar to the configuration etc. shall be included. This is the same also about the above-mentioned numeric value and the range.
[0037]
[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained in detail based on a drawing. In addition, what has the same function in the complete diagram for explaining the gestalt of operation attaches the same sign, and explanation of the repeat is omitted. Moreover, it does not repeat on the principle of explanation of the portion the same [except] or same when especially required.
[0038] The semiconductor integrated circuit equipment of this operation gestalt is the DRAM-logic mixed loading LSI in which DRAM (Dynamic Random Access Memory) and the logical circuit were formed on the same semiconductor substrate. The manufacture method of this LSI is explained in order of a process using drawing 1 - drawing 30 . In addition, in each cross section explaining the manufacture

respectively, and the so-called adoption of the dual gate CMOS (or it is also called CMIS (Complementary Metal Insulator Semiconductor)) structure which uses both both as a surface channel type is advanced.
[0017] In this case, when depositing a silicon nitride film at the process after gate electrode formation since there is a possibility of p type impurity in the gate electrode which consisted of p type polycrystal silicon (boron) being spread in a semiconductor substrate (well) through a gate oxide film, and fluctuating the threshold voltage of MISFET if heat treatment hot at the process after gate electrode formation is added, it is required that the pyrolysis temperature of source gas should be lowered.
[0018] Moreover, although it is necessary to form shallowly the pn junction which constitutes the source and a drain in order to raise the operating characteristic of MISFET which turned minutely, if heat treatment hot at the process after the source and drain formation is added, since the impurity of the source and a drain field will be spread and pn junction will spread, when depositing a silicon nitride film at the process after the source and drain formation, it is required that the pyrolysis temperature of source gas should be lowered.
[0019] However, if the pyrolysis temperature of source gas is lowered since the elevated temperature of about 800 degrees C or more is needed in order to dissociate completely the Si-H combination in silane system gas, and the N-H combination in ammonia gas, the Si-H combination and the N-H combination containing hydrogen of non-maceration will be incorporated so much in a silicon nitride film, and the fall of transistor characteristics which are pointed out with the aforementioned conventional technology will be invited.
[0020] As the cure, the proposal to which the hydrogen content of a silicon nitride film is reduced, and the proposal which understands the inside of silane system gas by perfect by enlarging RF power of plasma are also made by carrying out plasma decomposition of the source gas which uses comparatively the plasma CVD equipment which can form membranes at low temperature (about 400 degrees C), and does not contain hydrogen in a molecule. However, when a plasma CVD method is applied to the process immediately after gate electrode formation, in order that the front face and gate insulator layer of a substrate may receive the damage of plasma, we are anxious about the fall of transistor characteristics. Moreover, a plasma CVD method is difficult to deposit the silicon nitride film of desired thickness on the crevice between detailed gate electrodes, since the membranous coverage property is low compared with heat CVD.
[0021] The purpose of this invention has pattern density in offering the technology in which the thickness difference of the silicon nitride film in a **** field and a dense field can be reduced, in case pattern density deposits a silicon nitride film in heat CVD on the semiconductor wafer which has a **** field and a dense field.
[0022] The purpose of this invention is to offer the technology which can form a silicon nitride film with few hydrogen contents, without giving a thermal load to a transistor.
[0023] Other purposes of this invention are to offer the technology which can form a silicon nitride film with few hydrogen contents, without giving a plasma damage to a transistor.
[0024] Other purposes of this invention are to offer the technology which can form a silicon nitride film with a good step coverage, without giving a thermal load and a plasma damage to a transistor.
[0025] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.
[0026]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0027] The manufacture method of the semiconductor integrated circuit equipment of this invention includes the following processes.
(a) Introduce into the heat-treatment section the source gas containing the 1st gas which has silicon in a molecule, and the 2nd gas which has nitrogen in a molecule. The process which heat-treats the aforementioned source gas at the temperature more than the above 1st and the pyrolysis temperature of the 2nd gas, (b) Process which deposits the 1st insulator layer which makes a silicon nitride film a principal component on the principal plane of the semiconductor wafer which supplied the gas containing the decomposition product of the above 1st generated in the aforementioned heat-treatment section, and the 2nd gas to the membrane formation processing section, and was maintained at temperature lower than the pyrolysis temperature of the aforementioned source gas.
[0028] The manufacture method of the semiconductor integrated circuit equipment of this invention

silicon fluorides / sufficient for, and] them him is indicated. Moreover, before putting these two gas into a reaction vessel, after mixing as a method of supplying these excited gas to a substrate within a different reserve tub from a reaction vessel prepared for mixture of these gas, the method of supplying to a reaction vessel is indicated.

[0008] In manufacture of the TFT which used polycrystal silicon as a semiconductor region, in case JP,11-46000,A (Sakamoto) forms a gate insulator layer and a layer-insulation film on a polycrystal silicon film, it is indicating the technology reduce the amount of over etching of a polycrystal silicon film at the process which forms the contact hole which carries out dry etching of the insulator layer two-layer [these], and reaches a polycrystal silicon thin film, by constituting a gate insulator layer from a silicon-oxide film, and constituting a layer-insulation film from a silicon nitride film.

[0009] Moreover, in this official report, a lower layer silicon nitride film with high hydrogen content and hydrogen content constitute the above-mentioned layer insulation film from a low upper silicon nitride film. If hydrogen content of a lower layer silicon nitride film is made high, since a lot of hydrogen will be supplied into a polycrystal silicon film, the crystal defect of a polycrystal silicon film decreases and transistor characteristics improve. On the other hand, if the hydrogen content of the upper silicon nitride film is lessened, it is precise, and since a film with few pinholes is obtained, the isolation voltage of a transistor will improve.

[0010] The above-mentioned two-layer silicon nitride film from which hydrogen content differs is continuously deposited using plasma CVD equipment. The lower layer silicon nitride film with high hydrogen concentration makes temperature low (250 degrees C), and deposits a substrate, hydrogen concentration makes substrate temperature high (390 degrees C), and the low upper silicon nitride film accumulates.

[0011] By making into -three or less 0.6x1021 atom/cm the Si-H join total amount in the silicon nitride film used as a layer insulation film or a passivation film, JP,9-289209,A (Sonoda et al.) suppresses generating of the electron trap in a gate oxide film or a tunnel oxide film, and is indicating the technology which prevents threshold change of a transistor. The above-mentioned silicon nitride film is deposited by the plasma CVD method using the gas which has Si-H combination like a mono silane (SiH4) or a dichloro silane (Si2H6).

[0012] JP,2000-340562,A (Ito et al.) has pointed out the problem of negative bias temperature instability (Negative Bias Temperature Instability;NBTI) that change the threshold voltage of MISFET and the life of a device product becomes short under the influence of the hydrogen contained in the silicon nitride film used for the last protective coat (final passivation film) etc.

[0013] As a cure which suppresses property change of the device by the hydrogen in a silicon nitride film, this official report made Si-N combination main structure, made Si-NH2 combination ******, and has proposed using a silicon nitride film from which the integrated intensity of an Si-N bond-strength peak becomes 1000 or more times of the integrated intensity of a Si-NH2 bond-strength peak in FTIR (Fourier Transform Infrared Spectro-photo; Fourier transform type infrared spectrophotometer).

[0014] In addition, it is related with the CVD furnace using general remote plasma etc. A Japanese patent public presentation official report (correspondence U.S. application number 08 / 570058; U.S. filing date of application 95.12.11), for example, JP,9-181055,A, JP,10-154703,A (correspondence U.S. application number 08 / 748883; U.S. filing date of application 96.11.13), JP,10-154706,A (correspondence U.S. application number 08 / 746631; U.S. filing date of application 96.11.13), JP,10-163184,A (correspondence U.S. application number 08 / 748960; U.S. filing date of application 96.11.13), JP,10-178004,A (correspondence U.S. application number 08 / 748095; U.S. filing date of application 96.11.13), JP,10-189467,A (correspondence U.S. application number 08 / 748094; U.S. filing date of application 96.11.13), It is indicated by JP,10-256244,A (correspondence U.S. application number 08 / 747830; U.S. filing date of application 96.11.13), JP,11-74097,A (correspondence U.S. application number 08 / 839007; U.S. filing date of application 97.4.23), etc.

[0015]

[Problem(s) to be Solved by the Invention] The silicon nitride film used at the formation process of self aryne contact etc. has usually deposited silane system gas like a mono silane (SiH4) or a dichloro silane (Si2H6), and ammonia gas using the hot-wall type batch-type heat CVD system made to pyrolyze at an elevated temperature.

[0016] However, MISFET which is recently and which turned minutely constitutes n type polycrystal silicon and the gate electrode of p-channel type MISFET for the gate electrode of n channel type MISFET from p type polycrystal silicon as a cure which prevents the fall of threshold voltage,

implementation. Concentration of containing-in film immediately after membrane formation hydrogen can be more preferably made into three or less 0.5x1021 atoms/cm three or less 1x1021 atoms/cm three or less 2x1021 atoms/cm by this, and it is **.

[0102] Next, as shown in drawing 49 , control gate electrode 77c (word line WL) of the poly metal structure which serves as 71f of floating-gate electrodes which consist of polycrystal silicon 71 from the W film 75, the WNX film 74, and the polycrystal silicon film 73 is formed by using a photoresist film (not shown) as a mask and carrying out dry etching of a silicon nitride film 76, the W film 75, the WNX film 74, the polycrystal silicon film 73, the ONO film 72, and the polycrystal silicon film 71

[0103] Next, as shown in drawing 50 , the n-type-semiconductor field 70 which constitutes the source and the drain of MISFET is formed. the n-type-semiconductor field 70 -- p type -- the substrate 1 after carrying out the ion implantation of the n type impurity (for example, arsenic (As)) to a well 3 -- about 900 degrees C -- heat-treating -- the above-mentioned n type impurity -- p type -- it forms by making it spread in a well 3

[0104] Next, after washing the front face of a substrate 1, as shown in drawing 51 , a silicon nitride film 79 is deposited on a substrate 1. A silicon nitride film 79 is deposited using CVD system 100 of the gestalt 1 of the aforementioned implementation, or CVD system 200 of the gestalt 2 of the aforementioned implementation. Thereby, concentration of containing-in film immediately after membrane formation hydrogen can be more preferably made into three or less 0.5x1021 atoms/cm three or less 1x1021 atoms/cm three or less 2x1021 atoms/cm.

[0105] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of operation, it cannot be overemphasized by this invention that it can change variously in the range which is not limited to the gestalt of the aforementioned implementation and does not deviate from the summary.

[0106] Generally, the memory LSI, such as DRAM and a flash memory, includes the memory mat and the circumference circuit in one chip. Among these, although MISFET(s) which constitute a memory cell are arranged very densely in order that a memory mat may realize large-scale-ization of storage capacity, compared with a memory mat, as for a circumference circuit, MISFET(s) are arranged at a non-dense. Therefore, when the gate electrode of MISFET is formed on a wafer, as a result of generating a field (circumference circuit) **** in the pattern density of a gate electrode, and a dense field (memory mat), in each of two or more chip fields divided on the wafer, the phenomenon in which the thickness of a wrap silicon nitride film differs on a circumference circuit and a memory mat generates a gate electrode.

[0107] If the above problems (ununiformity of thickness) arise, by carrying out dry etching of the silicon nitride film Form a sidewall spacer in the side attachment wall of the gate electrode of a memory mat, and the side attachment wall of the gate electrode of a circumference circuit, or When a contact hole is formed by self-adjustment to a gate electrode or an isolation field, Since even the front face of not only the thin silicon nitride film that deposited on the memory mat the thick silicon nitride film deposited on the circumference circuit when it **********ed completely but its ground (a gate oxide film and substrate) will be deleted, the property of MISFET which constitutes a memory cell will deteriorate.

[0108] Since CVD system 100 of the gestalt 1 of the aforementioned implementation or CVD system 200 of the gestalt 2 of operation is supplied on the surface of a wafer after it decomposes source gas nearly completely in the exterior of a chamber beforehand, even when a field **** in the pattern density of a gate electrode and a dense field exist, it can form the silicon nitride film of the uniform thickness independent of the roughness and fineness of a gate electrode pattern.

[0109]

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated by this application is explained briefly.

[0110] Since a silicon nitride film with few hydrogen contents can be formed according to one mode of the invention in this application, without giving a thermal load to a transistor, the NBTI life of a device can be raised.

[0111] Since a silicon nitride film with few hydrogen contents can be formed according to other modes of the invention in this application, without giving a plasma damage to a transistor, the NBTI life of a device can be raised.

[Translation done.]

then, the wet etching using fluoric acid -- n+ type semiconductor region (the source --) After removing the gate insulator layer 10 of each front face of a drain 18 and p+ type semiconductor region (the source, drain) 19, Deposit Co film by the sputtering method on a substrate 1, and at the silicide reaction by heat treatment 11d of gate electrodes, After forming Co silicide layer 45 in each front face of 11e and n+ type semiconductor region (the source, drain) 18 and p+ type semiconductor region (the source, drain) 19, unreacted Co film is removed by wet etching. Of the process so far, n channel type MISFETQn and p-channel type MISFETQp which constitute Logic LSI are formed.
[0092] Next, as shown in drawing 37 , the silicon nitride film 46 of about 50nm of thickness is deposited in CVD on the principal plane of a substrate 1. This silicon nitride film 46 is deposited using aforementioned CVD system 200 used for deposition of a silicon nitride film 29. Membrane formation conditions are the same as the membrane formation conditions of a silicon nitride film 46 mentioned above, and good. Moreover, you may deposit a silicon nitride film 29 and a silicon nitride film 46 using CVD system 100 of the gestalt 1 of the aforementioned implementation.
[0093] Next, after depositing the silicon-oxide film 47 on source gas by the plasma CVD method using oxygen and the tetrapod ethoxy silane at the upper part of a silicon nitride film 46 as shown in drawing 38 for example, contact holes 48-51 are formed in the upper part of n+ type semiconductor region (the source, drain) 18 and p+ type semiconductor region (the source, drain) 19 by using a photoresist film (not shown) as a mask and carrying out dry etching of the silicon-oxide film 47 and the silicon nitride film 46 one by one.
[0094] The dry etching of the above-mentioned silicon-oxide film 47 is used for the stopper of etching of a silicon nitride film 46, and is performed on the conditions to which the etch rate of the silicon-oxide film 47 becomes large rather than the etch rate of a silicon nitride film 46. Moreover, the etch rate performs etching of a silicon nitride film 46 on the conditions which become larger than the etch rate of the silicon-oxide film 7 embedded in the isolation slot 4.
[0095] Next, as shown in drawing 39 , patterning of the metal film deposited on the upper part of the silicon-oxide film 47 is carried out, and the 1st-layer wiring 52-55 is formed.
[0096] (Gestalt 3 of operation) The semiconductor integrated circuit equipment of this operation gestalt is a flash memory. Hereafter, an example of the manufacture method of this flash memory of this is explained in order of a process using drawing 40 - drawing 52.
[0097] first, it is shown in drawing 40 -- as -- the same method as the gestalt 1 of the aforementioned implementation -- the principal plane of a substrate 1 -- the isolation slot 4 and p type -- after forming a well 8 and the gate insulator layer 10, as shown in drawing 41 and drawing 42 , the polycrystal silicon film 71 of 70nm - about 100nm of thickness is deposited in CVD on a substrate 1 On the polycrystal silicon film 71, n type impurity, for example, Lynn (P), is doped in the deposition process. Or after depositing the polycrystal silicon film of a non dope, you may dope n type impurity with ion-implantation. The polycrystal silicon film 71 is used as a floating-gate electrode of MISFET which constitutes a memory cell.
[0098] Next, as shown in drawing 43 and drawing 44 , the polycrystal silicon film 71 which has the band-like long flat-surface pattern which extends along the extension direction in the upper part of an active field is formed by using a photoresist film (not shown) as a mask and carrying out dry etching of the polycrystal silicon film 71.
[0099] Next, as shown in drawing 45 and drawing 46 , the ONO film 72 which consists of a silicon-oxide film, a silicon nitride film, and a silicon-oxide film is formed on the substrate 1 in which the polycrystal silicon film 71 was formed. The ONO film 72 is formed by being used as the 2nd gate insulator layer of MISFET which constitutes a memory cell, for example, depositing the silicon-oxide film of 5nm of thickness, the silicon nitride film of 7nm of thickness, and the silicon-oxide film of 4nm of thickness one by one in CVD on a substrate 1.
[0100] Next, as shown in drawing 47 and drawing 48 , n type polycrystal silicon film 73 which doped P (Lynn), the WNX film 74, the W film 75, and a silicon nitride film 76 are deposited on the upper part of the ONO film 67 one by one. The polycrystal silicon film 73, the WNX film 74, and the W film 75 are used as a control gate electrode (word line WL) of MISFET which constitutes a memory cell. Moreover, a silicon nitride film 76 is used as an insulator layer which protects the upper part of a control gate electrode. The polycrystal silicon film 73 can also constitute germanium (germanium) from a silicon film included just over or below 50% at the maximum.
[0101] A silicon nitride film 76 is deposited using CVD system 100 of the gestalt 1 of the aforementioned implementation, or CVD system 200 of the gestalt 2 of the aforementioned

channel type MISFET (Qn) which constitutes a part of logical circuit. Gate electrode 11e consists of a p type polycrystal silicon film with which boron was doped, and is used as a gate electrode of p-channel type MISFET (Qp) which constitutes a part of logical circuit.

[0083] next, it is shown in drawing 33 -- as -- p type -- a well 8 -- Lynn or an arsenic (As) -- an ion implantation -- carrying out -- the n type semiconductor field 15 of low high impurity concentration -- forming -- n type -- after carrying out the ion implantation of the boron to a well 9 and forming the p-type semiconductor field 16 of low high impurity concentration, the silicon nitride film 29 of about 50nm of thickness is deposited in CVD on the principal plane of a substrate 1 With this operation gestalt, this silicon nitride film 29 is deposited using the following equipments.

[0084] Drawing 34 is the schematic diagram showing the principal part of CVD system 200 used for deposition of a silicon nitride film 29. The remote plasma section (plasma treatment section) 202 which generates plasma using microwave etc. is formed in the exterior of a chamber 201 whose CVD system 200 is the membrane formation processing section. Source gas is introduced into a chamber 201 after being radically decomposed within this remote plasma section 202. The chamber 201 has the cold-wall structure of heating only the wafer 1 on a stage 203, like CVD system 100 of the gestalt 1 of the aforementioned implementation.

[0085] Thus, since above-mentioned CVD system 200 has the structure where the remote plasma section 202 which understands source gas by plasma, and the chamber 201 of each other were separated, the influence of plasma hardly attains to the wafer 1 on a stage 203. That is, since RF power can be set as high power (for example, frequency of 400kHz, 5kW or more of outputs) and decomposition of source gas can be promoted, without being anxious about the damage to a wafer 1, the Si-H combination and N-H combination in source gas can be made to dissociate nearly completely. Therefore, since it is not necessary to set the temperature of a wafer 1 as an elevated temperature, the thermal load of a device can be reduced. Furthermore, like existing plasma CVD equipment, since bias is not impressed to a wafer 1, high membrane formation of a step coverage is attained.

[0086] Although it is before and after 0 degree C, since it has a possibility of the throughput of membrane formation falling, or it being cooled as the intermediate field of the source gas generated within the remote plasma section 202 arrive at the front face of a wafer 1, and generating an impurity when the practical minimum temperature of the stage 203 at the time of membrane formation has the too low temperature of a stage 203, you should make it preferably 400 degrees C or more. The upper limit temperature of a stage 203 is the temperature of the upper limit permitted on the property of the device formed in the principal plane of a wafer 1, for example, in the case of the CMOS logic LSI of this operation gestalt, it is 700 degrees C - 750 degrees C.

[0087] The wall of a chamber 201 is held at 100 degrees C or less. Since the radical introduced into the chamber 201 by low-temperature-izing temperature of a wall stops being able to adhere to a wall easily, membrane formation speed becomes large. By this, even if it makes temperature of a stage 203 low, membranes can be formed in a short time, and the thermal load of a device is reduced further.

[0088] As for the pressure of source gas, it is desirable to consider as the range below 1.3kPa (10Torr), and to usually consider as 0.2kPa (1.5Torr) order more than 0.013kPa (0.1Torr).

[0089] The source gas used for formation of a silicon nitride film 14 Generally it is SiHyX (4-y) (X), such as the known source gas 4 currently used for formation of the silicon nitride film using reduced pressure CVD (LP-CVD) equipment, for example, SiH, and Si2H6. Halogens, such as F, Cl, Br, and I, and y can use what combined the silicon compound shown by 0, 1, 2, 3, or 4, and NH3, N2H4 or N2. When what combined the source gas, SiF4 and SiCl4, which does not contain hydrogen in a molecule among these silicon compounds, Si2Cl6, a silicon compound like SiBr4 and SiI4, and N2 is used, the hydrogen concentration in a silicon nitride film can be reduced further. [for example,]

[0090] By depositing a silicon nitride film 12 using above-mentioned CVD system 200, containing-in film immediately after membrane formation hydrogen concentration can be more preferably made into three or less 0.5x1021 atoms/cm three or less 1x1021 atoms/cm three or less 2x1021 atoms/cm, and the NBTI life of a device can be raised certainly.

[0091] Next, as shown in drawing 35 , sidewall spacer 29s is formed in each side attachment wall of the gate electrodes 11d and 11e by carrying out dry etching of the above-mentioned silicon nitride film 29 in different direction. next, it is shown in drawing 36 -- as -- p type -- a well 8 -- Lynn or an arsenic (As) -- an ion implantation -- carrying out -- n+ type semiconductor region (the source, drain) 18 of high high impurity concentration -- forming -- n type -- the ion implantation of the boron is carried out to a well 9, and p+ type semiconductor region (the source, drain) 19 of high high impurity concentration is formed

polycrystal silicon film of the upper part of the silicon-oxide film 35 is removed by dry etching (or chemical machinery polish).

[0077] Next, as shown in drawing 28 , after depositing a silicon nitride film 38 and depositing the silicon-oxide film 39 on the upper part of a silicon nitride film 38 in the upper part of the silicon-oxide film 35 in CVD continuously by CVD, a slot 40 is formed by carrying out dry etching of the upside silicon-oxide film 39 and upside silicon nitride film 38 of a through hole 36.

[0078] Next, as shown in drawing 29 , the lower electrode 41 which becomes the wall of a slot 40 from a polycrystal silicon film is formed. In order to form the lower electrode 41, after depositing on the interior of a slot 40, and the upper part of the silicon-oxide film 39 first the amorphous silicon film (not shown) which doped P (Lynn) in CVD, the unnecessary amorphous silicon film of the upper part of the silicon-oxide film 39 is removed by dry etching. Next, a silicon grain is grown up into the front face, while supplying a mono silane (SiH4) to the front face of an amorphous silicon film and heat-treating a substrate 1 continuously in reduced pressure atmosphere and polycrystal-izing an amorphous silicon film, after carrying out wet washing of the front face of the amorphous silicon film which remained in the interior of a slot 40 by the penetrant remover of a fluoric acid system. The lower electrode 41 which a front face becomes from the split-face-ized polycrystal silicon film by this is formed. Since the surface area is large, the polycrystal silicon film with which the front face was split-face-ized can increase the amount of stored charges of the capacitative element for information storage which turned minutely.

[0079] Next, as shown in drawing 30 , the capacitative element C for information storage which consists of the lower electrode 41, a capacity insulator layer 42, and an up electrode 43 is formed by forming the capacity insulator layer 42 which becomes the upper part of the lower electrode 41 formed in the interior of a slot 40 from 2OTa5 (tantalum oxide) film, and forming the up electrode 43 which becomes the upper part of the capacity insulator layer 42 from a TiN film. The film which makes a principal component the high dielectric or ferroelectric which has the crystal structure of perovskite types, such as others, PZT and PLT, PLZT, and PbTiO3, SrTiO3, BaTiO3, BST, SBT or Ta 2O5, or a compound perovskite [film / 2OTa5] type may constitute the capacity insulator layer 42 of the capacitative element C for information storage. The memory cell of DRAM which consists of capacitative element C for information storage connected to MISFETQt for memory cell selection and this in series according to the process so far is completed.

[0080] Although illustration is omitted, DRAM of this operation gestalt is completed by forming aluminum wiring about two-layer on both sides of the layer insulation film which becomes the upper part of the capacitative element C for information storage from a silicon-oxide film, and forming after that, the passivation film which becomes the upper part of aluminum wiring from the cascade screen of a silicon nitride film and a silicon-oxide film further. Since the silicon nitride film which constitutes some passivation films is deposited in thickness 1 micrometers or more, it is required that high membrane formation of a throughput should be performed. Moreover, it is required at the process after forming MISFETQt for memory cell selection, and the capacitative element C for information storage that membranes should be formed at low temperature. Therefore, not the CVD system shown in aforementioned drawing 10 but well-known batch-type plasma CVD equipment is used for the silicon nitride film which constitutes some passivation films, and it forms membranes at about 400-degree C low temperature.

[0081] (Gestalt 2 of operation) The semiconductor integrated circuit equipment of this operation gestalt is the CMOS-logic LSI. The manufacture method of this LSI is explained in order of a process using drawing 31 - drawing 39 .

[0082] first, it is shown in drawing 31 -- as -- the same method as the gestalt 1 of the aforementioned implementation -- a substrate 1 -- the isolation slot 4 and p type -- a well 8 and n type -- a well 9 is formed next, the thing for which a substrate 1 is oxidized thermally at about 800-850 degrees C as shown in drawing 32 after washing the front face of a substrate 1 by the wet etching using fluoric acid -- p type -- a well 8 and n type -- the pure gate insulator layer 10 is formed in each front face of a well 9, and the gate electrodes 11d and 11e are continuously formed in the upper part of the gate insulator layer 10 The gate electrodes 11d and 11e are formed by using a photoresist film as a mask and carrying out dry etching of the polycrystal silicon film, after depositing the polycrystal silicon film of 200nm - about 250nm of thickness and carrying out [upper part / of the gate insulator layer 10] the ion implantation of the n type impurity (Lynn) to some polycrystal silicon films continuously by CVD and carrying out the ion implantation of the p type impurity (boron) to other parts. 11d of gate electrodes consists of an n type polycrystal silicon film with which Lynn was doped, and they are used as a gate electrode of n

formation field, and the gate electrodes 11b and 11c are formed on the gate insulator layer 10 of a logical-circuit formation field. The gate electrodes 11a-11c consist of poly metal (Polymetal) structures which carried out the laminating of the WNX film 12 and the W film 13 to the upper part of the polycrystal silicon film 11. As shown in drawing 13 , gate electrode 11a of a DRAM formation field extends in the direction which intersects perpendicularly with the long side of the active field L, and constitutes a word line WL from fields other than the active field L. The gate length of gate electrode 11a and the interval with adjoining gate electrode 11a are 0.13-1.4 micrometers.

[0062] next, after removing the photoresist film 61, it is shown in drawing 14 -- as -- a photoresist film (not shown) -- a mask -- using -- p type -- a well 8 -- As (arsenic) -- an ion implantation -- carrying out -- n type -- by carrying out the ion implantation of the B (boron) to a well 9 p type of the both sides of the gate electrodes 11a and 11b -- a well 8 -- the n type semiconductor field 15 -- forming -- n type of the both sides of gate electrode 11c -- the p-type semiconductor field 16 is formed in a well 9

[0063] Next, as shown in drawing 15 , the silicon nitride film 17 of about 50nm of wrap thickness is deposited for the upper part and the side attachment wall of the gate electrodes 11a, 11b, and 11c. This silicon nitride film 17 is deposited using CVD system 100 used for deposition of the aforementioned silicon nitride film 14, and also makes membrane formation conditions (the kind and pressure of the temperature of a heater 104 and a stage 102, and source gas) the same as the membrane formation conditions of a silicon nitride film 14. Thereby, like the aforementioned silicon nitride film 14, while the hydrogen concentration in a film can obtain the low silicon nitride film 17 extremely, property change of the device by the thermal load can be suppressed certainly.

[0064] Drawing 16 is a graph which shows the result which evaluated the relation between the Si-H joint concentration in a wrap silicon nitride film, and a NBTI life (time for threshold voltage to shift 20mV) for the upper part and the side attachment wall of a gate electrode. The silicon nitride film used a mono silane (SiH_4) and ammonia (NH_3) for source gas, and deposited them using the commercial low pressure CVD system, and the Si-H joint concentration in a film was measured using the Fourier transform type infrared spectrophotometer (FTIR). Moreover, a mono silane (SiH_4) and nitrogen (N_2) were used for source gas, and evaluation with the same said of the silicon nitride film deposited using commercial plasma CVD equipment was performed.

[0065] Consequently, a NBTI life has the Si-H joint concentration in a silicon nitride film, and correlation, and falling in proportion to the 1.2nd power of Si-H joint concentration made it clear. From this, the NBTI life of a device can be certainly raised by making [the upper part of the gate electrodes 11a, 11b, and 11c] concentration of the hydrogen immediately after membrane formation into three or less 0.5x1021 atoms/cm for the wrap aforementioned silicon nitride film 14 and a side attachment wall more preferably three or less 1x1021 atoms/cm three or less 2x1021 atoms/cm in the case of the wrap silicon nitride film 17.

[0066] Next, as shown in drawing 17 , sidewall spacer (side-attachment-wall insulator layer) 17s is formed in the side attachment wall of the gate electrodes 11b and 11c of a logical-circuit formation field by covering the substrate 1 of a DRAM formation field by the photoresist film (not shown), and **********ing the silicon nitride film 17 of the circuit section in different direction. then, a photoresist film (not shown) -- a mask -- using -- p type of a logical-circuit formation field -- a well 8 -- As (arsenic) -- an ion implantation -- carrying out -- n type -- by carrying out the ion implantation of the B (boron) to a well 9 p type of the both sides of the gate electrodes 11a and 11b -- a well 8 -- n+ type semiconductor region (the source, drain) 18 -- forming -- n type of the both sides of gate electrode 11c -- p+ type semiconductor region (the source, drain) 19 is formed in a well 9 According to the process so far, n channel type MISFETQn and p-channel type MISFETQp which constitute a logical circuit are completed.

[0067] Next, as shown in drawing 18 , the layer insulation film 20 which consists of a spin-on glass film and a two-layer silicon-oxide film is formed in the upper part of the gate electrodes 11a-11c. In order to form the layer insulation film 20, the spin application of the spin-on glass film is carried out first at the upper part of the gate electrodes 11a-11c. Since the spin-on glass film is excellent in the gap philharmonic nature during detailed wiring compared with the silicon-oxide film deposited in CVD, even if it is the case that between gate electrode 11a (word line WL) of a DRAM formation field is very narrow, it can embed this crevice good. Next, after depositing a silicon-oxide film on the upper part of a spin-on glass film in CVD, by the chemical machinery grinding method, it grinds and flattening of this silicon-oxide film is carried out. Next, in order to repair a blemish with the detailed front face of the silicon-oxide film produced when ground by the chemical machinery grinding method (micro scratch),

the silicon-oxide film of a two-layer eye is deposited on the upper part of a silicon-oxide film in CVD.
[0068] Next, as shown in drawing 19 and drawing 20 , the layer insulation film 20 of the upper part of the n type semiconductor field 15 of a DRAM formation field is removed by the dry etching which used the photoresist film (not shown) as the mask. This etching is performed on conditions to which the etching rate of the layer insulation film 20 (a spin-on glass film and silicon-oxide film) to silicon nitride films 14 and 17 becomes large.
[0069] Then, the silicon nitride film 17 of the upper part of the n type semiconductor field 15 is removed by the dry etching which used the above-mentioned photoresist film as the mask, and contact holes 21 and 22 are formed by exposing the front face of the n type semiconductor field 15. The part separates from a contact hole 21 from the active field L, and it extends in the upper part of the isolation slot 4.
[0070] Etching of the above-mentioned silicon nitride film 17 is performed on conditions to which the etching rate of the silicon nitride film 17 to the silicon-oxide film 7 embedded in the isolation slot 4 becomes large, and it prevents from deleting the isolation slot 4 deeply. Moreover, a silicon nitride film 17 performs this etching on conditions on which it **********s in different direction, and it leaves a silicon nitride film 17 to the side attachment wall of gate electrode 11a (word line WL). The contact holes 21 and 22 which have a detailed path by this are formed by self-adjustment to gate electrode 11a (word line WL).
[0071] Next, a plug 23 is formed in the interior of contact holes 21 and 22 as shown in drawing 21 . In order to form a plug 23, dry etching deposits the low resistance polycrystal silicon film which doped P in CVD and removes the unnecessary polycrystal silicon film of the upper part of the layer insulation film 20 in the interior of contact holes 21 and 22, and the upper part of the layer insulation film 20 continuously.
[0072] Next, the source of low resistance and a drain are formed by heat-treating a substrate 1 in nitrogen-gas-atmosphere mind, and making the n type semiconductor field 15 diffuse P in the polycrystal silicon film which constitutes a plug 23. MISFETQt for memory cell selection is formed in a DRAM formation field at the process so far.
[0073] Next, as shown in drawing 22 and drawing 23 , after depositing the silicon-oxide film 24 on the upper part of the layer insulation film 20 in CVD, By carrying out dry etching of the silicon-oxide film 24 and its lower layer layer insulation film 20 of a logical-circuit formation field by the dry etching which used the photoresist film (not shown) as the mask A contact hole 25 is formed in the source of n channel type MISFETQn, and the upper part of a drain (n+ type semiconductor region 18), and a contact hole 26 is formed in the source of p-channel type MISFETQp, and the upper part of a drain (p+ type semiconductor region 13). Moreover, a through hole 27 is formed in the upper part of a contact hole 21 by **********ing the silicon-oxide film 24 of a DRAM formation field.
[0074] Next, as shown in drawing 24 and drawing 25 , after forming a plug 28 in the interior of the above-mentioned contact holes 25 and 26 and a through hole 27, a bit line BL is formed in the upper part of the silicon-oxide film 24 of a DRAM formation field, and wiring 30-33 is formed in the upper part of the silicon-oxide film 24 of a logical-circuit formation field.
[0075] After depositing a TiN film and W film on the upper part of the silicon-oxide film 24 including the interior of contact holes 25 and 26 and a through hole 27 in the sputtering method and CVD in order to form a plug 28 for example, unnecessary upside W film and the upside TiN film of the silicon-oxide film 24 are removed by the chemical machinery grinding method. Moreover, in order to form a bit line BL and wiring 30-33, after depositing W film on the upper part of the silicon-oxide film 24 by the sputtering method, patterning of the W film is carried out by the dry etching which used the photoresist film for the mask. As for a bit line BL, the source of MISFETQt for memory cell selection and a drain are electrically connected with on the other hand (n type semiconductor field 15) through a through hole 27 and a contact hole 21. Moreover, wiring 30 and 31 is electrically connected with the source of n channel type MISFETQn, and a drain (n+ type semiconductor region 18) through contact holes 25 and 25, and wiring 32 and 33 is electrically connected with the source of p-channel type MISFETQp, and a drain (p+ type semiconductor region 19) through contact holes 26 and 26.
[0076] Next, as shown in drawing 26 and drawing 27 , after depositing the silicon-oxide film 35 and carrying out dry etching of the silicon-oxide films 35 and 24 of the upper part of a contact hole 22 to the upper part of a bit line BL and wiring 30-33 continuously by CVD and forming a through hole 36, the plug 37 which consists of a polycrystal silicon film is formed in the interior of a through hole 36. In order to form a plug 37, after depositing on the interior of a through hole 36, and the upper part of the silicon-oxide film 35 in CVD the polycrystal silicon film which doped P (Lynn), the unnecessary